

Serial No. 10/760,599**Docket No. 200313613-1****REMARKS**

Claims 1-30 are currently pending in the subject application, and are presently under consideration. Claims 1-30 are rejected. Claims 18 and 23 have been amended to correct typographical errors. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Amendments to the Specification

The Related Applications section of the present application has been amended to replace the identified attorney docket numbers with the application serial numbers and to identify the common filing date of the identified applications.

II. Rejection of Claims 1-4, 9, 14, 16-17, 20, 23-24, and 29 under 35 U.S.C. 102(e)

Claims 1-4, 9, 14, 16-17, 20, 23-24, and 29 have been rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Number 2005/0251626 to Glasco. Applicant traverses this rejection for the following reasons.

The Office Action contends that Glasco anticipates the system of claim 1. Applicant respectfully disagrees with this contention. Claim 1 recites a system where a first node, which includes an ordering point for data, employs a write-back transaction associated with writing the data back to memory. Claim 1 also recites that the memory provides an acknowledgement to indicate that the ordering point for the data has migrated to the memory. Generally stated, the ordering point for the data migrates from the first node to the memory and the memory provides an acknowledgement to indicate that such ordering point migration has occurred.

In sharp contrast to claim 1, Glasco does not disclose that an ordering point can migrate from a node to memory, as recited in claim 1. Instead, Glasco employs memory controllers to act as serialization points for each memory line, but fails to disclose that any serialization point

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for a memory line can migrate. See Glasco at para. [0047] and [0127]. Significantly, even during an eviction or write transaction, such as during a write back to memory, a given memory controller remains the serialization point for the memory line before, during and after writing back to memory. See Glasco at para. [0137] and [0127]. Since Glasco fails to teach that an ordering point can migrate from a node to memory, as recited in claim 1, Glasco consequently also fails to teach that memory would provide any acknowledgement to indicate that the ordering point has migrated from the first node to the memory, as recited in claim 1. For example, what basis exists for memory to provide an acknowledgement to an event that simply does not occur in the system of Glasco?

Additionally, the Office Action appears to have misconstrued the teachings Glasco by contending that the modified write back message described in Glasco is provided in response to an acknowledgement provided by the memory indicating that the ordering point has migrated from the first node to the memory. In contrast to the contention in the Office Action, Glasco teaches the modified line of memory must first be written back to memory before the line is invalidated if the directory entry indicates that the line is in the "dirty" state in any of the remote caches. See Glasco at para. [0116], lines 4 to 8, and para. [0126]. As discussed above, Glasco taken in whole or part, fails to teach that an ordering point migrate for data migrates to memory, such that there can be no broadcasting of a write-back message by the first node in response to the acknowledgement provided by the memory, as recited in claim 1. For the reasons stated above, Applicant respectfully requests reconsideration and allowance of claim 1.

In contrast to claim 2, Glasco fails to teach or suggest that a cache lines has associated state that defines the cache line as a cache ordering point for the data prior to employing the write-back transaction (of claim 1). As discussed with respect to claim 1, Glasco teaches that a

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memory controller acts as a serialization point for a memory line (see para. [0045]-[0046]), but fails to teach that an associated state of a cache line defines the cache line as an ordering point for the data, as recited in claim 2. The reference to para. [0126] in the Office Action supports Applicant's conclusion since it is the home memory controller that is the serialization point. Therefore Glasco fails to teach claim 2. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 2.

Regarding claim 3, Glasco fails to disclose the at least one other node provides a response the first node acknowledging receipt of the write-back message broadcast by the first node. Instead Glasco teaches the home memory controller receives a dirty copy of the memory line, writes the line back to memory and notifies the originator of the transaction that the transaction is complete. See Glasco para. [0126]. However, in this example of Glasco, the originator of the transaction (the cache coherence controller in the home cluster - see para. [0124]) does not broadcast a write back message, as recited in claim 1. Instead the other node, i.e. home memory controller, notifies the originator of the transaction that the transaction is complete. Glasco Para. [0126]. The notification is not taught as being provided for acknowledging a write-back message that was broadcast by a first node, as recited in claim 3. Accordingly, Applicant respectfully requests withdraw of the rejection of claim 3 as well as claims 4-7 that depend from claim 3.

Additionally, regarding claim 4, the Office Action cites para. [0121]-[0123] and [0127] to support its contention that Glasco discloses claim 4. In sharp contrast to claim 4, however, nothing in the cited sections of Glasco or elsewhere in Glasco is there a disclosure that the first node (which employs the write back transaction - of claim 1) maintains the transaction active until the first node receives responses from the at least one other node to the write-back message

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that was broadcast by the first node. First, Applicant submits that there is no discussion in the Office Action as to what parts of Glasco might correspond to claimed subject matter. Second, the sections of Glasco being relied upon fail to teach that any message or notification is broadcast by the originator of the transaction (the cache coherence controller). Because Glasco fails to teach each and every element of claim 4, claim 4 is not anticipated. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 4.

The Office Action contends that Glasco discloses the system of claim 9 citing the reasons for the rejections of claims 1 and 2. The Applicant respectfully disagrees with this contention. Similar to the reasoning stated in support of claim 1, there is no teaching in Glasco of a write-back request to transfer an ordering point from cache of the first processor to memory, especially not in response to the write-back request recited in claim 9. Instead, as discussed above, the ordering point for a line of memory remains in the memory controller - before, during and after the memory line is written back to memory. See Glasco at para. [0127] and [0137].

Consequently, Glasco also fails to teach or even suggest the other acknowledgement and broadcasting of requests that occur in response to the write-back request provided by the first processor as recited in claim 9. As mentioned above, it appears that the Office Action has mischaracterized the teachings of Glasco as it might pertain to claim 9. Accordingly, the Applicant respectfully requests reconsideration and allowance of claim 9, as well as claims 10-15 that depend from claim 9.

Claim 14 is further patentable over Glasco for substantially similar reasons to those discussed above with respect to claim 2.

Claim 16, which is written in means-plus-function format is patentable for reasons similar to those provided in support of claims 1 and 9, Glasco fails to disclose claim 16. For

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example, as discussed above, Glasco teaches that the home memory controller acting as the serialization point receives a "dirty" copy of the memory line, if one exists, performs a NOP, and writes the line back to memory. Glasco Para. [0126]. The write-back as taught in Glasco transfers a memory line to memory, but fails to migrate any ordering point, especially migration of an ordering point from an associated cache to memory. See Glasco Para. [0126] and [0127]. Accordingly, the Applicant respectfully requests reconsideration and allowance of claim 16 as well as claims 17-22 that depend from claim 16.

Claim 23 has been amended to correct a typographical error. For reasons similar to those provided in support of claims 1, 9, and 16, Glasco fails to anticipate claim 23. For example, the system of Glasco in teaching eviction of a remotely cached "dirty" memory line, Glasco fails to disclose that a write-back request from a processor node is provided to transfer an ordering point to memory. See, *e.g.*, Glasco abstract, Para. [0116], Para. [0120] to [0127]. Moreover, there is no basis to conclude that Glasco teaches or even suggests that the originator of the write back also provides a source broadcast message to other nodes in response to an acknowledging receipt of the write-back request at the memory. Instead, the system in Glasco appears to only issue probes from the home memory controller in response to the originating sized write request, in response to which the local nodes respond by returning any dirty copy of the memory line and invalidating the corresponding entries in their caches. See Glasco at para. [0124]-[0125]. For these reasons, Applicant respectfully requests reconsideration and allowance of claim 23 as well as claims 24-30 that depend from claim 23.

Additionally, claims 24 and 29 are patentable for substantially the same reasons as presented above with respect to claims 3 and 2, respectively.

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III. Rejection of Claims 5-6, 8, 10-11, 13, 15, 18-19, 21-22, 25-28, and 30 under 35 U.S.C. 103(a)

Claims 5-6, 8, 10-11, 13, 15, 18-19, 21-22, 25-28, and 30 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Glasco in view of U.S. Patent Publication No. 2003/0217236 to Rowlands ("Rowlands"). Applicant traverses this rejection for the following reasons.

Claims 5-6, 8, 10-11, 13, 15, 18-19, 21-22, 25-28, and 30 are patentable for at least the same reasons discussed above with respect to the base claims and any intervening claims from which they depend. Additionally, the addition of Rowlands does not cure the deficiencies of Glasco as applied to these claims. As discussed below, it appears that when the Office Action incorporates rationale previously applied as its basis to support rejection of other claims, the rationale being incorporated to reject several claims does not appear relevant to such claims.

Additionally, the reliance on Rowlands (para. [0057], [0065] and [0113]) does not provide a basis to conclude that one of ordinary skill in the art would seek to modify the system of Glasco to provide the system of claim 5. Significantly, Rowlands does not teach or suggest that a transaction would be retried in response to recognizing a conflict. Instead, Rowlands simply discloses that the approach taught in Rowlands can use an interconnect that may or may not support retry. Accordingly, the combined teachings of Rowlands and Glasco fail to provide sufficient motivation to create the system of claim 5.

With regard to claim 6, the Office Action again relies on para. [0127]. However, this section has no teaching or suggestion that any third node can recognize a conflict. Instead, as discussed above, para. [0127] describes some particular functionality of the home memory

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controller and the role it plays in avoiding race conditions during a write back of a memory line. See Glasco at para. [0127]. Reconsideration and allowance of claim 6 are respectfully requested.

Applicant respectfully submits that the cited section of Rowlands, as well as its teachings as a whole, appear irrelevant to what is recited in claim 8. For example, there is nothing in Rowlands, individually or in combination with Glasco, that provides any suggestion of allocating an entry in a miss address file that is maintained until responses have been received from all other nodes in the system to the write-back message broadcast by the first node. The failure of any explanation as to the relevance of Rowlands to claim 8 supports Applicant's position. Therefore, Applicant respectfully requests reconsideration and allowance of claim 8.

Applicant respectfully submits that claims 10, 11, and 13 be allowed for the reasons discussed above with respect to claims 5, 6, and 8, respectfully.

Regarding claim 15, as discussed above, Glasco fails to teach or suggest that a state of a cache line can define a cache line as an ordering point. Instead, Glasco teaches that the serialization point (memory controller or a cache controller) for a memory line is independent of the state of a given line of memory. See Glasco at para. [0045]-[0046], [0127] and [0137]. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 15.

Claim 18 has been amended to depend from claim 17 and is patentable for at least the same reasons as claim 17. Additionally, the rationale relied upon in the Office Action (the same as applied to claim 5) fails to provide a prima facie case of unpatentability. For example, since claim 5 does not recite the same subject matter as claim 18 (e.g., the means for retiring an outstanding transaction....), the incorporation of rationale provided in the Office Action is insufficient as a basis for rejecting claim 18. Applicant, therefore, respectfully requests allowance of claim 18.

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Applicant respectfully submits that claims 19 and 27 be allowed for the reasons discussed above with respect to claims 5.

Claims 21 should further be allowed for at least the same reasons as claim 15.

Claim 25 is patentable for the reasons provided above with respect to claim 4.

Claim 26 is patentable for the reasons provided above with respect to claim 18.

Claim 28 is patentable for the reasons provided above with respect to claim 6.

IV. Rejection of Claims 7 and 12 under 35 U.S.C. 103(a)

Claims 7 and 12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Glasco in view of Rowlands and further in view of U.S. Patent No. 6,138,218 to Arimilli ("Arimilli"). Applicant traverses this rejection for the following reasons.

The further addition of Arimilli does not cure the deficiencies of Glasco in view of Rowlands as applied to claims from which claims 7 and 12 depend. Additionally, the approach taught by Arimilli is not that a given node retries its own source broadcast request employing a forward progress protocol, as recited in claim 7. In contrast, Arimilli teaches that the responding cache 114 takes action, such as altering the coherency state associated with requested cache item 208 in its own memory or initiating a push operation to write (modified) requested cache item 208 to system memory. See Arimilli at Col. 5, lines 32-51, and Abstract. That is, the cache 116 that issues the retry (206) does not retry its transaction using any forward progress protocol, but instead it is the responding cache (114) that initiates the action to enable an intervention response to proceed. See Arimilli at Col. 5, lines 32-51. For these reasons, Applicant respectfully requests reconsideration and allowance of claim 7.

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Claim 12 is patentable for substantially similar reasons to those discussed with respect to claim 7.

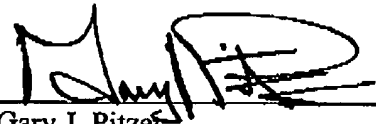
CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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